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10/038,291	01/02/2002	Syamal Kumar Lahiri	11042-004	7028
20583	7590	04/27/2005	EXAMINER	
JONES DAY 222 EAST 41ST ST NEW YORK, NY 10017			BEREZNY, NEMA O	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary

Application No.

10/038,291

Applicant(s)

LAHIRI ET AL.

Examiner

Nema O. Berezny

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 November 2004.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 17-60 is/are pending in the application.
- 4a) Of the above claim(s) 17-25 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 26-60 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to Applicant's Amendment filed 11-30-04, which has been entered and considered. Applicant's Petition to revive the previously abandoned instant application has been granted. Claims 17-60 are currently pending, with claims 17-25 withdrawn; cancellation of claims 1-16 is acknowledged.

Claim Objections

Claims 34, 37 and 55 are objected to because of the following informalities: in line 1 (claim 34), line 2 (claim 37), and lines 9 and 13 (claim 55), delete "brining" and insert --bringing-- thereto. Appropriate correction is required.

Claim 43 is objected to because of the following informalities: in line 2, delete "wore" and insert --wire-- thereto. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 26-28, 33, and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Takushima (6,454,159). Takushima discloses a method of constructing

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an electrical contact on a first electrical component, comprising the steps of: on an electronic chip including an interconnection surface, the interconnection surface including a plurality of exposed contact pads (col.2 lines 55-58) and a non-wetting surface between the contact pads (implied for a semiconductor device), fabricating on each of a portion of or all of the contact pads a protruding electrically conducting core having a solder wettable surface (col.2 lines 55-58); and bringing the entire interconnection surface in contact with molten solder, thereby depositing solder on all of the cores to form solder bumps thereon and leaving a substantial absence of solder between cores (col.2 line 58 – col.3 line 6; col.4 lines 51-60) **[claim 26]**. Takushima also discloses wherein the electrically conducting core includes a metal stud (col.2 lines 59-61) **[claim 27]**; wherein said fabricating a protruding electrically conducting core is performed by bonding a wire to a contact pad (col.3 lines 25-45) **[claim 28]**; wherein the step of bringing the entire interconnection surface in contact with molten solder is performed by dipping the interconnection surface into a bath of molten solder (col.2 line 58 – col.3 line 6; col.4 lines 51-60) **[claim 33]**; and wherein the electrically conducting core is formed from a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys (col.5 lines 10-14) **[claim 40]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 29 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima as applied to claims 26 and 28 above. However, Takushima is silent as to the diameter of a wire to form the conducting core and the pitch of the contact pads. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima as applied to claims 26 and 27 above, and further in view of Lin (6,440,835). Takushima does not disclose coining the metal studs. However, Takushima would look to one such as Lin for improved mounting because Lin discloses coining the metal studs after fabrication on the contact pads (col.14 lines 18-21). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the coining of Lin with the method of Takushima in order to flatten the head to improve mounting said chip to another component.

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima as applied to claims 26 and 27 above, and further in view of Azdasht et al. (6,043,985). Takushima does not disclose stacking a plurality of studs by wire bonding.

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However, Takushima would look to one such as Azdasht for flexible connectors because Azdasht discloses stacking a plurality of studs by wire bonding (col.4 lines 51-64). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the plurality of studs of Azdasht with the method of Takushima in order to form flexible connectors with independent connector bodies (Azdasht - col.1 line 66 – col.2 line 10).

Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima as applied to claim 26 above, and further in view of Gutierrez (6,395,983). Takushima does not disclose wave soldering. However, Takushima would look to one such as Gutierrez for mass fabrication because Gutierrez discloses wherein the step of bringing the entire interconnection surface in contact with molten solder is performed through a wave soldering process (col.7 lines 16-18). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the wave soldering of Gutierrez with the method of Takushima in order to mass fabricate several solder bumps or leads simultaneously, thereby saving time and costs.

Claims 32 and 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima as applied to claim 26 above, and further in view of Cotte et al. (6,281,105). Takushima does not disclose a specific solder bump dimension, or wafer fabrication, or repeating contacting the molten solder, or connecting said chip to another component. However, Takushima would look to one such as Cotte for conventional

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fabrication, mass fabrication, an improved electrical connection, and forming a chip assembly. Cotte discloses wherein the formed solder bumps have a dimension of 75 microns or less without any bridging in-between (col.3 lines 61-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the solder bump dimension of Cotte with the method of Takushima in order to save time and costs by using conventionally used materials (Cotte - col.3 lines 61-67) **[claim 32]**.

Cotte discloses wherein the step of bringing the entire interconnection surface in contact with molten solder is performed on a plurality of electronic chips on the same wafer (col.4 lines 4-7), wherein it is implied that following the step of bringing the entire interconnection surface in contact with molten solder, Cotte discloses dicing the wafer into individual chips. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the wafer fabrication of Cotte with the method of Takushima in order to mass produce said bringing in contact step, thereby saving time and costs **[claims 36, 37, 42]**.

Cotte discloses repeating the contact of the interconnection surface with molten solder to increase the size of the solder bumps (col.4 lines 14-26). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the repeating contact of Cotte with the method of Takushima in order to increase the amount of solder particles adhering to the bump, thereby improving the electrical connection (Cotte – col.4 lines 24-26) **[claim 38]**.

Cotte discloses electrically connecting the produced chip of claim 26 to a second electronic component, the second electronic component having corresponding solderable contacts positioned to mate with the contacts of the first electrical component, the method further comprising the steps of: mating the first and second electronic components such that the corresponding contacts of both the first and second electronic components are brought into proximal alignment (col.5 lines 3-13); and applying heat to make an electrical connection between the corresponding contacts of the first and second electronic components using the solder of the solder bumps of the first electronic component (col.5 lines 18-23). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the mating and applying of Cotte with the method of Takushima in order to form a chip assembly (Cotte – col.5 lines 23-24) **[claim 39]**.

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima as applied to claim 26 above, and further in view of Abbott et al. (6,337,445). Takushima does not disclose a conducting core coated with another material. However, Takushima would look to one such as Abbott for a cheaper core material because Abbott discloses wherein the electrically conducting core is coated with a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys (col.8 lines 19-26, 35-38). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the coated core of Abbott with the method of Takushima in order to provide a conducting core of a cheaper

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material, such as copper that can be covered with a more expensive material, such as a noble metal that would provide oxidation resistance (Abbott – col.8 lines 35-38).

Claims 43, 48, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima in view of Cotte as applied to claim 42 above. Takushima also discloses wherein said fabricating a protruding stud is performed by bonding a wire to a contact pad (col.3 lines 25-45) **[claim 43]**; wherein the step of bringing the entire interconnection surface in contact with molten solder is performed by dipping the interconnection surface into a bath of molten solder (col.2 line 58 – col.3 line 6; col.4 lines 51-60) **[claim 48]**; and wherein the electrically conducting core is formed from a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys (col.5 lines 10-14) **[claim 53]**.

Claims 44 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima in view of Cotte as applied to claims 42 and 43 above. However, Takushima is silent as to the diameter of a wire to form the stud and the pitch of the contact pads. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578; 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima in view of Cotte as applied to claim 42 above, and further in view of Lin (6,440,835). Takushima and Cotte do not disclose coining the metal studs. However, Takushima and Cotte would look to one such as Lin for improved mounting because Lin discloses coining the metal studs after fabrication on the contact pads (col.14 lines 18-21). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the coining of Lin with the method of Takushima and Cotte in order to flatten the head to improve mounting said chip to another component.

Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima in view of Cotte as applied to claim 42 above, and further in view of Azdasht et al. (6,043,985). Takushima and Cotte do not disclose stacking a plurality of studs by wire bonding. However, Takushima and Cotte would look to one such as Azdasht for flexible connectors because Azdasht discloses stacking a plurality of studs by wire bonding (col.4 lines 51-64). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the plurality of studs of Azdasht with the method of Takushima and Cotte in order to form flexible connectors with independent connector bodies (Azdasht - col.1 line 66 – col.2 line 10).

Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima in view of Cotte as applied to claim 42 above, and further in view of Gutierrez (6,395,983). Takushima and Cotte do not disclose wave soldering. However,

Takushima and Cotte would look to one such as Gutierrez for mass fabrication because Gutierrez discloses wherein the step of bringing the entire interconnection surface in contact with molten solder is performed through a wave soldering process (col.7 lines 16-18). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the wave soldering of Gutierrez with the method of Takushima and Cotte in order to mass fabricate several solder bumps or leads simultaneously, thereby saving time and costs.

Claims 47 and 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima in view of Cotte as applied to claim 42 above. Takushima does not disclose a specific solder bump dimension, or repeating contacting the molten solder, or connecting said separated chip to another component. However, Takushima would look to one such as Cotte for conventional fabrication, an improved electrical connection, and forming a chip assembly. Cotte discloses wherein the formed solder bumps have a dimension of 75 microns or less without any bridging in-between (col.3 lines 61-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the solder bump dimension of Cotte with the method of Takushima in order to save time and costs by using conventionally used materials (Cotte - col.3 lines 61-67) **[claim 47]**.

Cotte discloses repeating the contact of the interconnection surface with molten solder to increase the size of the solder bumps (col.4 lines 14-26). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to

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use the repeating contact of Cotte with the method of Takushima in order to increase the amount of solder particles adhering to the bump, thereby improving the electrical connection (Cotte – col.4 lines 24-26) [**claim 51**].

Cotte discloses electrically connecting the produced chip of claim 42 to a second electronic component, the second electronic component having corresponding solderable contacts positioned to mate with the contacts of the separated chip, the method further comprising the steps of: mating the separated chip and second electronic components such that the corresponding contacts of both the first and second electronic component such that the corresponding contacts of both are brought into proximal alignment (col.5 lines 3-13); and applying heat to make an electrical connection between the contacts of the separated chip and second electronic component using the solder of the solder bumps of the separated chip (col.5 lines 18-23). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the mating and applying of Cotte with the method of Takushima in order to form a chip assembly (Cotte – col.5 lines 23-24) [**claim 52**].

Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima in view of Cotte as applied to claim 42 above, and further in view of Abbott et al. (6,337,445). Takushima and Cotte do not disclose a conducting core coated with another material. However, Takushima and Cotte would look to one such as Abbott for a cheaper core material because Abbott discloses wherein the electrically conducting core is coated with a material selected from the group consisting of gold, copper, silver,

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platinum, palladium and nickel and their alloys (col.8 lines 19-26, 35-38). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the coated core of Abbott with the method of Takushima and Cotte in order to provide a conducting core of a cheaper material, such as copper that can be covered with a more expensive material, such as a noble metal that would provide oxidation resistance (Abbott – col.8 lines 35-38).

Claims 55-56 and 58-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima (6,454,159) in view of Cotte et al. (6,281,105), and further in view of Lin (6,440,835). Takushima discloses a method of constructing an electrical contact on a first electrical component, comprising the steps of: on an electronic chip including an interconnection surface, the interconnection surface including a plurality of exposed contact pads (col.2 lines 55-58) and a non-wetting surface between the contact pads (implied for a semiconductor device), fabricating on each of a portion of or all of the contact pads a protruding metal stud having a solder wettable surface (col.2 lines 55-58) by bonding a wire to the contact pads (col.3 lines 25-45); and bringing the entire interconnection surface in contact with molten solder through a solder bath or wave solder process, thereby depositing solder on all of the studs to form solder bumps thereon and leaving a substantial absence of solder between studs (col.2 line 58 – col.3 line 6; col.4 lines 51-60). However, Takushima does not disclose a specific solder bump dimension, or wafer fabrication. Takushima would look to one such as Cotte for conventional fabrication and mass fabrication because Cotte discloses wherein the

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formed solder bumps have a dimension of 75 microns or less without any bridging in-between (col.3 lines 61-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the solder bump dimension of Cotte with the method of Takushima in order to save time and costs by using conventionally used materials (Cotte - col.3 lines 61-67). Cotte also discloses wherein the step of bringing the entire interconnection surface in contact with molten solder is performed on a plurality of electronic chips on the same wafer (col.4 lines 4-7), wherein it is implied that following the step of bringing the entire interconnection surface in contact with molten solder, Cotte discloses dicing the wafer into individual chips.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the wafer fabrication of Cotte with the method of Takushima in order to mass produce said bringing in contact step, thereby saving time and costs.

Takushima and Cotte do not disclose coining the metal studs. However, Takushima and Cotte would look to one such as Lin for improved mounting because Lin discloses coining the metal studs after fabrication on the contact pads (col.14 lines 18-21).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the coining of Lin with the method of Takushima and Cotte in order to flatten the head to improve mounting said chip to another component.

Takushima, Cotte, and Lin are silent as to the pitch of the contact pads. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a

claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990) **[claim 55]**.

Takushima, Cotte, and Lin are silent as to the diameter of a wire to form the conducting core. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990) **[claim 56]**.

Takushima does not disclose repeating contacting the molten solder. However, Takushima would look to one such as Cotte for an improved electrical connection because Cotte discloses repeating the contact of the interconnection surface with molten solder to increase the size of the solder bumps (col.4 lines 14-26). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the repeating contact of Cotte with the method of Takushima in order to increase the amount of solder particles adhering to the bump, thereby improving the electrical connection (Cotte – col.4 lines 24-26) **[claim 58]**.

Takushima also discloses wherein the electrically conducting core is formed from a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys (col.5 lines 10-14) **[claim 59]**.

Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima in view of Cotte and Lin as applied to claim 55 above, and further in view of Azdasht et al. (6,043,985). Takushima, Cotte, and Lin do not disclose stacking a plurality of studs by wire bonding. However, Takushima, Cotte, and Lin would look to one such as Azdasht for flexible connectors because Azdasht discloses stacking a plurality of studs by wire bonding (col.4 lines 51-64). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the plurality of studs of Azdasht with the method of Takushima, Cotte, and Lin in order to form flexible connectors with independent connector bodies (Azdasht - col.1 line 66 – col.2 line 10).

Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takushima in view of Cotte and Lin as applied to claim 55 above, and further in view of Abbott et al. (6,337,445). Takushima, Cotte, and Lin do not disclose a conducting core coated with another material. However, Takushima, Cotte, and Lin would look to one such as Abbott for a cheaper core material because Abbott discloses wherein the electrically conducting core is coated with a material selected from the group consisting of gold, copper, silver, platinum, palladium and nickel and their alloys (col.8 lines 19-26, 35-38). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the coated core of Abbott with the method of Takushima, Cotte, and Lin in order to provide a conducting core of a cheaper material, such as

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copper that can be covered with a more expensive material, such as a noble metal that would provide oxidation resistance (Abbott – col.8 lines 35-38).

Response to Arguments

Applicant's arguments with respect to claims 26-60 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O. Berezny whose telephone number is (571) 272-1686. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NB

A handwritten signature in black ink, appearing to read "Nema O. Berezny", with a long, sweeping horizontal stroke extending to the right.